INTEL 8259A Programmable Interrupt Controller

The 8259A is a programmable interrupt controller specially designed to work with Intel microprocessor 8080, 8085A, 8086, 8088. The main features of 8259A programmable interrupt controller are given below:

1) It can handle eight interrupt inputs. This is equivalent to providing eight interrupt pins on the processor in place of one INTR (in 8085A)/INT(in 8086) pin.
2) The chip can vector an interrupt request anywhere in the memory map from 0000H to FFFFH in 8085A microprocessor. However, all the eight interrupts are spaced at an interval of either four or eight locations. This eliminates the major drawback of 8085A interrupts in which all interrupts are vectored to memory location on page 00_H i.e., TRAP, RST7.5, RST6.5 and RST5.5 are vectored to memory locations 0024H, 003CH, 0034H and 002CH respectively.
3) It can resolve eight levels of interrupt priorities in a variety of modes. The priorities of interrupts can be changed under running condition. Some of the desired lower priority interrupts may be allowed to be acknowledged during the service of higher priority interrupts.
4) Each of the interrupt requests can be masked individually similar to RST7.5, RST6.5 and RST5.5 interrupts of 8085A.
5) The status of pending interrupts, in service interrupts, and masked interrupts can be read at any time similar to RST interrupts of 8085A.

6) The chip can be programmed to accept interrupt requests either as level triggered or edge triggered interrupt request unlike your RST interrupts where some are edge triggered and some are level triggered. However, all interrupts must be either level triggered or edge triggered.

7) If required, nine 8259As can be cascaded in a master-slave configuration mode to handle 64 interrupt inputs. In this case, the interrupting devices send their interrupt requests either to slave 8259A or to master 8259A directly. The slave 8259As send their interrupt to master interrupt request inputs and the master will send a single interrupt to microprocessor interrupt pin INTR/INT.

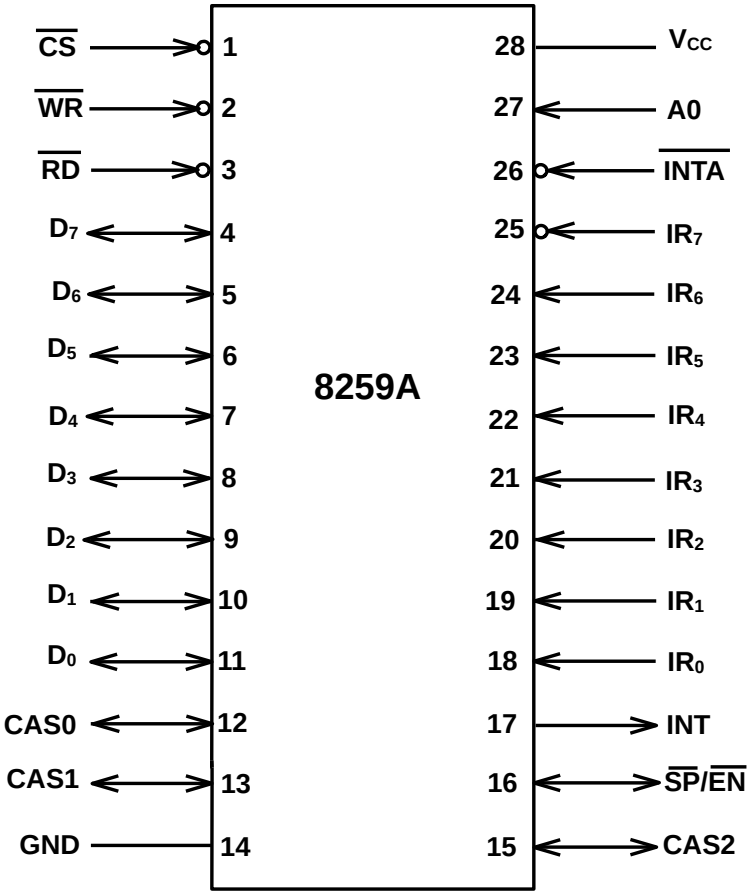

Fig.11.2 Pin Configuration of Intel 8259A

The 8259 A is contained in a 28 dual-in-line package that requires only +5V supply voltage. The 8259A is upward compatible with 8259. The main difference between the two is that the 8259A can be used with Intel 8086/8088 processor. It also includes additional features such as level triggered mode, buffered mode and automatic end of interrupt mode.

The pin diagram and internal block diagram of PIC is shown in figure. The pins are defined as follows:

$\overline{\text{CS}}$ (Chip Select signal): To access this chip, chip select signal $\overline{\text{CS}}$ is made low. A LOW on this pin enables $\overline{\text{RD}}$ & $\overline{\text{WR}}$ communication between the CPU and the 8259A. This signal is made LOW by decoding the addresses assigned to this chip. Therefore, this pin is connected to address bus through the decoder logic circuit. Interrupt acknowledge functions to transfer the control to interrupt service subroutine are independent of $\overline{\text{CS}}$.

$\overline{\text{WR}}$ (Write signal): A low on this pin. When $\overline{\text{CS}}$ is low enables the 8259 A to accept command words from CPU.

$\overline{\text{RD}}$ (Read signal): A low on this pin when $\overline{\text{CS}}$ is low enables this 8259A to release status (pending interrupts or in-service interrupts or masked interrupts) on to the data bus for the CPU. The status includes the contents of IMR (interrupt mask register) or ISR (interrupt service register) or IRR (interrupt request register) or a priority level.

D_7-D_0 (Data Bus): Bidirectional data bus. Control, status and interrupt vector information is transferred via this data bus. This bus is connected to BDB of 8085A.

CAS_2-CAS_0 (Cascade lines): The CAS_{2-0} lines form a local 8259A bus to control multiple 8259As in master-slave configuration, i.e., to identify a particular slave 8259A to be accessed for transfer of vector information. These pins are automatically set as output pins for master 8259A and input pins for a slave 8259A once the chips are programmed as master or slave.

$\overline{SP}$/ $\overline{EN}$ (Salve Program/Enable Buffer): This is a dual function pin. When the chip is programmed in buffered mode, the pin can be used as an output and when not in the buffered mode it is used as an input. In non-buffered mode it is used as an input pin to determine whether the 8259A is to be used as a master ($\overline{SP}$/ $\overline{EN}$ = 1) or as a slave ($\overline{SP}$/ $\overline{EN}$ = 0). In buffered mode, normally data bus buffers are used. These buffers need to be enabled or disabled during transfer of vector information depending upon whether 80259A is connected before the buffer or after the buffer. To disable/enable the data bus transceivers (buffers) when data are being transferred from the 8259A to the CPU, this pin is made low or high.

INT (Interrupt output): This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin (INTR). In case of master-slave

configuration, the interrupt pin of slave 8259A is connected to interrupt request input of master 8259A.

$\overline{\textbf{INTA}}$ (Interrupt Acknowledge): This pin is used to enable 8259A interrupt vector data on the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

IR_0-IR_7 (Interrupt Request inputs): These are asynchronous interrupt request input pins. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged. (Edge triggered mode) or just by a high level on an interrupt request input (Level triggered mode).

A_0 (A_0 address line): This pin acts in conjunction with the $\overline{RD}$, $\overline{WR}$ & $\overline{CS}$ pins. It is used by the 8259A to send various command words from the CPU and to read the status. It is normally connected to the CPU A_0 address line. Two addresses are assigned/ reserved in the I/O address space for each 8259A in the system- one with A_0 =0 is called even address and other with A_0 = 1 is called odd address.

Functional Description:

The 8259A (PIC) has eight interrupt request inputs – IR_7 - IR_0. The 8259A uses its INT output to interrupt the 8085A via INTR pin. The 8259A receives interrupt acknowledge pulses from the μp at its $\overline{INTA}$ input. Vector address, used by the 8085A to transfer control to the service subroutine of the interrupting device, is provided by the

8259A on the data bus. The 8259A is a programmable device that must be initialized by command words sent by the microprocessor. After initialization the 8259A mode of operation can be changed by operation command words from the microprocessor.

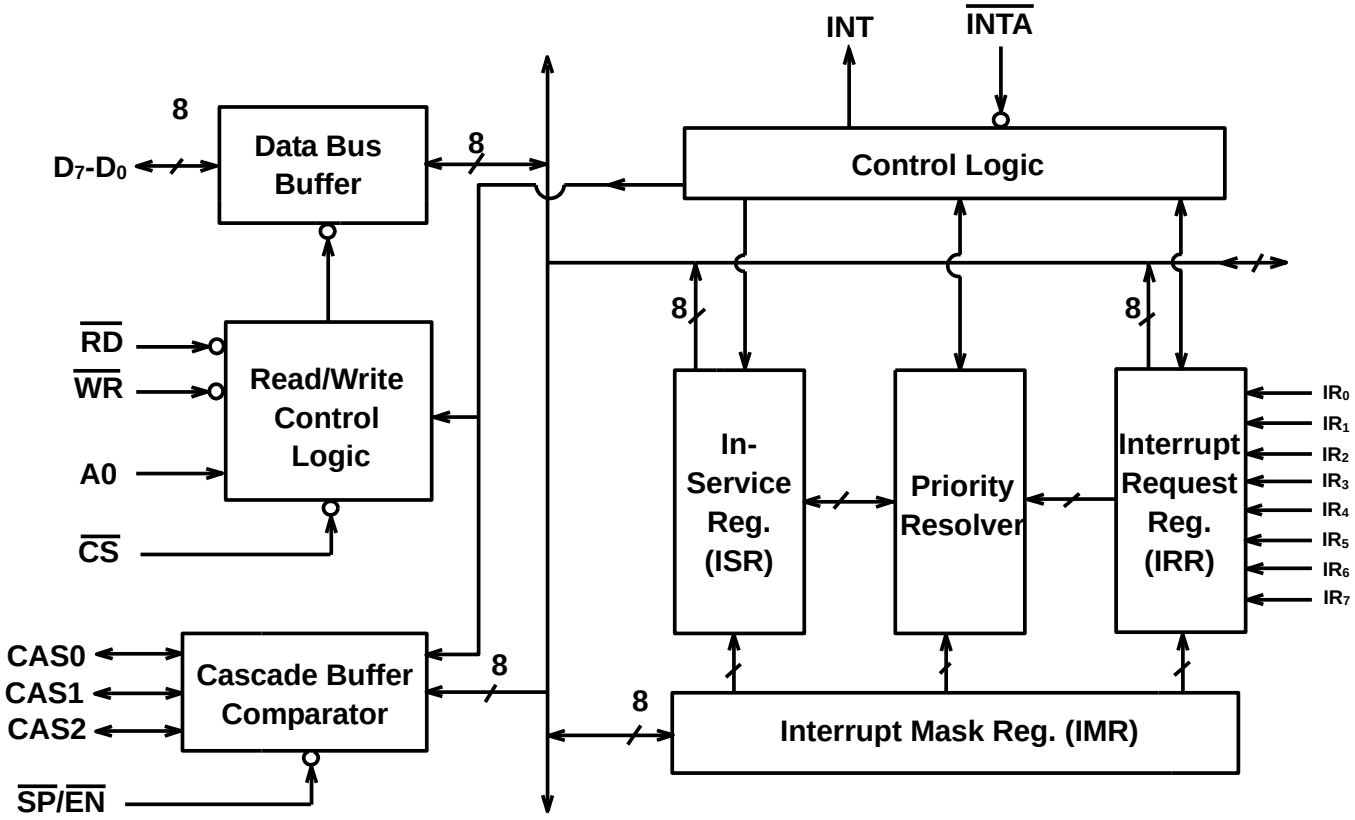

Fig.11.3 Internal Structure of 8259A

The descriptions of various blocks are given below:

Data bus buffer:

This 3- state, bidirectional 8-bit buffer is used to interface the 8259A to the system data bus. Control words and status information from the microprocessor to PIC and from PIC to microprocessor respectively, are transferred through the data bus buffer.

Read/Write & Control Logic: The function of this block is to accept output commands sent from the CPU. It contains the initialization command word (ICW) registers and operation command word (OCW) registers which store the various control formats for device operation. This function block also allows the status of 8259A to be transferred to the data bus.

Interrupt Request Register (IRR): Interrupt request register (IRR) stores all the interrupt inputs that are requesting service. It is an 8-bit register – one bit for each interrupt request. Basically, it keeps track of which interrupt inputs are asking for service. If an interrupt input is unmasked, and has an interrupt signal on it, then the corresponding bit in the IRR will be set. The content of this register can be read to know the status of pending interrupts.

Interrupt Mask Register (IMR): The IMR is used to disable (Mask) or enable (Unmask) individual interrupt request inputs. This is also an 8-bit register. Each bit in this register corresponds to the interrupt input with the same number. The IMR operates on the IRR. Masking of higher priority input will not affect the interrupt request lines of lower priority. To unmask any interrupt the corresponding bit is set '0'.

In-service Register (ISR): The in-service register keeps track of which interrupt inputs are currently being serviced. For each input that is currently being serviced the corresponding bit of in-service register (ISR) will be set. In 8259A, during the service of an interrupt request, if another higher priority interrupt becomes active, it will be

acknowledged and the control will be transferred from lower priority interrupt service subroutine (ISS) to higher priority ISS. Thus, more than one bit of ISR will be set indicating the number of interrupts being serviced.

Each of these 3-registers can be read as status register.

Priority Resolver: This logic block determines the priorities of the interrupts set in the IRR. It takes the information from IRR, IMR and ISR to determine whether the new interrupt request is having highest priority or not. If the new interrupt request is having the highest priority, it is selected and processed. The corresponding bit of ISR will be set during interrupt acknowledge machine cycle.

Cascade Buffer/Comparator: This function block stores and compares the IDs of all 8259A's in the system. The associated 3-I/O lines (CAS_2-CAS_0) are outputs when 8259A is used as a master and are inputs when 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS_{2-0} lines. The slave 8259As compare this ID with their own programmed ID. Thus selected 8259A will send its pre-programmed subroutine address on to the data bus during the next one or two successive $\overline{INTA}$ pulses.